# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 09-266229
(43)Date of publication of application : 07.10.1997

(51)Int.Cl. H01L 21/60
H01L 21/56
H01L 23/29
H01L 23/31
H05K 1/18

(21)Application number : 08-073674
(22)Date of filing : 28.03.1996

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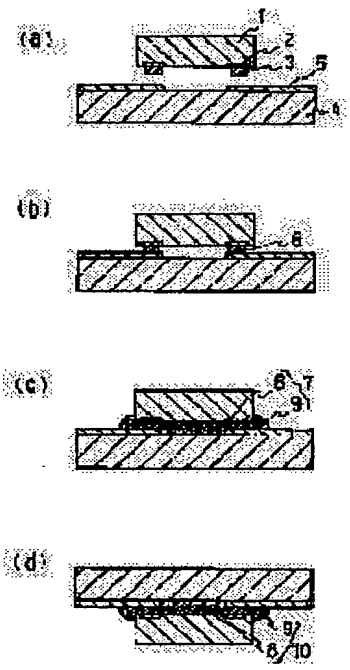
## (54) PACKAGING METHOD OF SEMICONDUCTOR DEVICE AND PACKAGED STRUCTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent thermal stress from being produced owing to thermal contraction of a resin component, by filling a gap between a semiconductor device and a circuit board with the liquid resin mixture containing an inorganic filler, and hardening the resin mixture in the state where the inorganic mixture is located in the vicinity of a small thermal expansion coefficient member.
SOLUTION: A gap between a semiconductor device 1 and a circuit board 4 is filled with a liquid resin mixture 7. The circuit board 4 is turned over and is heated at temperature of about 150° C to harden the liquid resin mixture 7. The liquid resin mixture 7 contains at least resin 8 and an inorganic filler 9, in which a ratio of the resin 8 and the inorganic filler 9 is adjusted such that a thermal expansion coefficient of the resin mixture 10 after being hardened is coincident with that of a junction 6 of a conductive bonding agent. Further, the hardening is performed in the state wherte the inorganic filler 9 is displaced to the side of a small thermal expansion coefficient semiconductor device 1.




LEGAL STATUS

[Date of request for examination] 03.07.1998
[Date of sending the examiner's decision of rejection]
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number] 2930186

[Date of registration] 21.05.1999
[Number of appeal against examiner's decision of rejection]
[Date of requesting appeal against examiner's decision of rejection]
[Date of extinction of right]

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CLAIMS

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[Claim(s)]

[Claim 1] The mounting approach of the semiconductor device characterized by to have the process which is the mounting approach of a semiconductor device of mounting a semiconductor device in the circuit board by face down, and mounts said semiconductor device in said circuit board, the process filled up with the liquefied resin constituent which contains resin and an inorganic filler in the gap of said semiconductor device and said circuit board, and the process which hardens said resin constituent in the condition that said inorganic filler is located near the small member of a coefficient of thermal expansion.

[Claim 2] The mounting approach of the semiconductor device according to claim 1 which hardens said resin constituent in the condition that said inorganic filler is located near said circuit board when the coefficient of thermal expansion of said semiconductor device is larger than the coefficient of thermal expansion of said circuit board.

[Claim 3] The mounting approach of the semiconductor device according to claim 1 which hardens said resin constituent in the condition that said inorganic filler is located near said semiconductor device when the coefficient of thermal expansion of said semiconductor device is smaller than the coefficient of thermal expansion of said circuit board.

[Claim 4] The mounting approach of a semiconductor device according to claim 1, 2, or 3 of using the specific gravity difference of said resin in said liquefied resin constituent, and said inorganic filler as an approach of positioning said inorganic filler.

[Claim 5] The mounting approach of a semiconductor device according to claim 3 of turning said circuit board over and using the specific gravity difference of said resin and said inorganic filler as an approach of locating said inorganic filler near said semiconductor device.

[Claim 6] The mounting approach of the semiconductor device of five given in any 1 term from claim 1 using the property in which the viscosity of said resin in said liquefied resin constituent falls rapidly in the state of an elevated temperature as an approach of positioning said inorganic filler.

[Claim 7] The mounting approach of a

semiconductor device according to claim 6 of performing positioning of said inorganic filler, and hardening of said liquefied resin constituent at the same process.

[Claim 8] The mounting approach of the semiconductor device of seven given in any 1 term from claim 1 which mounts said semiconductor device in said circuit board using a solder bump.

[Claim 9] The mounting approach of the semiconductor device of seven given in any 1 term from claim 1 which mounts said semiconductor device in said circuit board using electroconductive glue.

[Claim 10] The mounting approach of the semiconductor device of seven given in any 1 term from claim 1 which mounts said semiconductor device in said circuit board using a projection electrode and electroconductive glue.

[Claim 11] The mounting object of the semiconductor device characterized by being in the condition in which the semiconductor device was mounted in the circuit board, was equipped with the resin constituent which contains resin and an inorganic filler in the gap of said semiconductor device and said circuit board, and said inorganic filler in said resin constituent was located near the small member of a coefficient of thermal expansion.

[Claim 12] The mounting object of the semiconductor device according to claim 11 with which it has said resin constituent from which a coefficient of thermal expansion changes perpendicularly to said circuit board.

[Claim 13] The mounting object of the semiconductor device according to claim 11 or 12 which is in the condition in which said inorganic filler in said resin constituent was located near said circuit board when the coefficient of thermal expansion of said semiconductor device is larger than the coefficient of thermal expansion of said circuit board.

[Claim 14] The mounting object of the semiconductor device according to claim 11 or 12 which is in the condition in which said inorganic filler in said resin constituent was located near said semiconductor device when the coefficient of thermal expansion of said semiconductor device is smaller than the coefficient of thermal expansion of said circuit board.

[Claim 15] The mounting object of the semiconductor device according to claim 12, 13, or 14 whose average of the vertical coefficient of thermal expansion to said circuit board of said resin constituent corresponds with the value of the vertical coefficient of thermal expansion to said circuit board of the connection part of said semiconductor device and said circuit board mostly.

[Claim 16] The mounting object of the semiconductor device according to claim 15 with which it has said resin constituent with which the rate of said

resin and said inorganic filler was adjusted so that the average of the vertical coefficient of thermal expansion to said circuit board of said resin constituent and the value of the vertical coefficient of thermal expansion to said circuit board of the connection part of said semiconductor device and said circuit board may be mostly in agreement.

[Claim 17] The mounting object of the semiconductor device of 16 given in any 1 term from claim 11 using an inorganic filler spherical as said inorganic filler in said resin constituent.

[Claim 18] The mounting object of the semiconductor device of 17 given in any 1 term from claim 11 by which said semiconductor device is mounted in said circuit board using the solder bump.

[Claim 19] The mounting object of the semiconductor device of 17 given in any 1 term from claim 11 by which said semiconductor device is mounted in said circuit board using electroconductive glue.

[Claim 20] The mounting object of the semiconductor device of 17 given in any 1 term from claim 11 by which said semiconductor device is mounted in said circuit board using a projection electrode and electroconductive glue.

[Claim 21] The mounting object of the semiconductor device of 20 given in any 1 term from claim 11 equipped with said semiconductor device with which coefficients of thermal expansion differ, and said circuit board.

## DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the mounting approach of a semiconductor device, and its mounting object in detail about a semiconductor device.

[0002]

[Description of the Prior Art] When it mounts a semiconductor device to up to the circuit board conventionally, the approach by soldering is common. However, by the miniaturization of the package of a semiconductor device, and the increment in the number of connection terminals, spacing between connection terminals becomes narrow and it is becoming difficult gradually to cope with it with the conventional soldering technique in recent years.

[0003] So, recently, the approach of aiming at a miniaturization and efficient use of a component-side product is invented by carrying out direct attachment of the naked semiconductor device on the circuit board. There is the following as the example.

[0004] First, in case the approach connects a semiconductor device to the circuit board electrically, it carries out the laminating of the solder layer beforehand formed of the vacuum evaporationo film of an adhesion metal or a diffusion

prevention metal, and plating on the terminal electrode of a semiconductor device. And next, the face down of the semiconductor device which has the above electrode structure is carried out on the circuit board, it heats to an elevated temperature and welding of the solder on the terminal electrode of a semiconductor device is carried out to the connection electrode of the circuit board.

[0005] According to this approach, it can carry out by putting connection in block, and the mounting structure by this approach has further the description that the mechanical strength after connection is strong. Therefore, it is supposed that it is this approach an effective approach.

[0006] Moreover, in order to secure the stability of the joint by solder, the mounting object of the semiconductor device which carried out the resin seal of between a semiconductor device and the circuit boards is indicated by the U.S. Pat. No. 5121190 specification.

[0007] Hereafter, the mounting approach and mounting object of the conventional semiconductor device are explained. Drawing 5 is the important section sectional view of the mounting object of the semiconductor device in the conventional technique. In drawing 5 , the joint according [ accord / the circuit board and 5 / a connection electrode / 1 / 2 / a semiconductor device and / 13 ] to solder in the terminal electrode of a semiconductor device 1 and 4 and 14 are closure resin.

[0008] In this conventional technique, the semiconductor device 1 with which the solder bump was formed on the terminal electrode 2 is first carried in the position of the connection terminal 5 of the circuit board 4 by face down. Next, it heats to a 200-300-degree C elevated temperature, melting of the solder bump on the terminal electrode 2 is carried out, and welding is carried out to the connection terminal 5. By carrying out like this, a semiconductor device 1 and the circuit board 4 are connected by the joint 13 by solder. Then, the gap of a semiconductor device 1 and the circuit board 4 is filled up with liquefied closure resin 14, and heat hardening is carried out at the temperature of about 150 degrees C. According to the above process, the mounting object which closed the semiconductor device 1 by closure resin 14 can be acquired.

[0009]

[Problem(s) to be Solved by the Invention] However, in the mounting object of the above conventional semiconductor device, by change of the environmental temperature at the time of using the mounting object of this semiconductor device, the thermal stress by the difference of the coefficient of thermal expansion of a semiconductor device 1 and the circuit board 4 will arise, and the joint 13 by solder will be joined by that thermal stress. Moreover, when

using especially the mounting object of this semiconductor device in an elevated-temperature field, also in the closure resin 14 with which the gap of a semiconductor device 1 and the circuit board 4 is filled up, the new thermal stress by thermal expansion will arise, and the joint 13 by solder will be joined by this thermal stress. Therefore, in this conventional mounting object, since all of such thermal stress join the joint 13 by solder, the dependability of the electrical installation of a semiconductor device 1 and the circuit board 4 gets worse.

[0010] In order to avoid such thermal stress, it is necessary to secure the stability of the joint 13 by solder using what has a coefficient of thermal expansion small as closure resin 14 (it is a match to the coefficient of thermal expansion of the joint 13 according to solder still more preferably). As such (a coefficient of thermal expansion is small) closure resin 14, what carried out content of the inorganic filler about 40 to 75% of the weight (still more preferably about 50 - 60 % of the weight) can be considered in closure resin 14.

[0011] However, although it will solve about the thermal stress of the joint 13 by the solder which works perpendicularly (it only says also "perpendicularly" hereafter.) to the circuit board if such closure resin 14 (what has such a small coefficient of thermal expansion that it agrees in the coefficient of thermal expansion of the joint 13 by solder) is used The circuit board is met and it is in parallel (it is hereafter called "the direction of a flat surface".). About the thermal stress produced according to the difference of the coefficient of thermal expansion of the semiconductor device 1 and the circuit board 4 which work, it is unsolvable. If about it and such closure resin 14 are used, the thermal stress of the direction of a flat surface will increase further.

[0012] Increase of such thermal stress of the direction of a flat surface is produced when coefficients of thermal expansion with the joint 13, the semiconductor device 1, and the circuit board 4 by solder differ greatly. That is, since it cannot be made to agree with the coefficient of thermal expansion of a semiconductor device 1 and the circuit board 4 even if it makes the coefficient of thermal expansion of closure resin 14 agree in the joint 13 of solder, increase of thermal stress takes place according to the difference of the coefficient of thermal expansion. Therefore, the thermal stress produced according to the difference of the coefficient of thermal expansion of the direction of these flat surfaces joins the joint 13 by solder, and worsens the dependability of the electrical installation of a semiconductor device 1 and the circuit board 4.

[0013] This invention was made in order to solve such a technical problem, and it

aims at offering the mounting approach of the mounting object of a reliable semiconductor device, and the semiconductor device for obtaining this.

[0014]

[Means for Solving the Problem] This invention for attaining the above-mentioned purpose is the mounting approach of a semiconductor device of mounting a semiconductor device in the circuit board by face down, and is characterized by to have the process which mounts said semiconductor device in said circuit board, the process which fills up the gap of said semiconductor device and said circuit board with the liquefied resin constituent containing resin and an inorganic filler, and the process which hardens said resin constituent in the condition that said inorganic filler is located near the small member of a coefficient of thermal expansion.

[0015] By carrying out like this, the inclination of a coefficient of thermal expansion will occur in said resin constituent after hardening which intervenes between said semiconductor devices and said circuit boards between the part which has the distribution condition of said inorganic filler, i.e., said inorganic filler, and the part which is not. Therefore, a perpendicular direction and the direction of a flat surface can prevent effectively generating of the thermal stress by heat expansion of said resin constituent by how said inorganic filler is distributed.

[0016] Moreover, when the coefficient of thermal expansion of said semiconductor device is larger than the coefficient of thermal expansion of said circuit board, it is desirable to harden said resin constituent in the condition that said inorganic filler is located near said circuit board. Since said inorganic filler has the effectiveness of raising thermal conductivity, according to said mounting approach, heat conduction over said circuit board improves, and the difference of the coefficient of thermal expansion of said semiconductor device and said circuit board is eased here. therefore, generating of the thermal stress said resin constituent after hardening will have the inclination of a coefficient of thermal expansion perpendicularly, and according to heat expansion of said resin constituent -- a perpendicular direction and the direction of a flat surface -- it can prevent -- said semiconductor device and said circuit board -- dependability -- it can mount highly.

[0017] Furthermore, when the coefficient of thermal expansion of said semiconductor device is smaller than the coefficient of thermal expansion of said circuit board, it is desirable to harden said resin constituent in the condition that said inorganic filler is located near said semiconductor device. By carrying out like this, heat conduction over said

semiconductor device improves, the difference of the coefficient of thermal expansion of said semiconductor device and said circuit board is eased, and the direction of a flat surface can be prevented perpendicularly [ generating / of the thermal stress by heat expansion of said resin constituent ].

[0018] Moreover, as an approach of positioning said inorganic filler, the method of using the specific gravity difference of said resin in said liquefied resin constituent and said inorganic filler, the method of using the property in which the viscosity of said resin in said liquefied resin constituent falls rapidly in the state of an elevated temperature, etc. are desirable. Furthermore, the method of turning said circuit board over and using the specific gravity difference of said resin and said inorganic filler as an approach of locating said inorganic filler near said semiconductor device, is also desirable. Moreover, the method of performing positioning of said inorganic filler and hardening of said liquefied resin constituent at the same process is also desirable.

[0019] Furthermore, the approach of mounting said semiconductor device in said circuit board using a solder bump, the method of mounting said semiconductor device in said circuit board using electroconductive glue, the method of mounting said semiconductor device in said circuit board using a projection electrode and electroconductive glue, etc. are desirable.

[0020] Moreover, said inorganic filler in said resin constituent is characterized by being in the condition to which the semiconductor device was mounted in the circuit board by the semiconductor device concerning this invention, and it was equipped with the resin constituent which contains resin and an inorganic filler in the gap of said semiconductor device and said circuit board, and the mounting object was located in it near the small member of a coefficient of thermal expansion. Furthermore, it is desirable to have said resin constituent from which a coefficient of thermal expansion changes perpendicularly to said circuit board. Moreover, when it being in the condition in which said inorganic filler in said resin constituent was located near said circuit board when the coefficient of thermal expansion of said semiconductor device is larger than the coefficient of thermal expansion of said circuit board, and the coefficient of thermal expansion of said semiconductor device are smaller than the coefficient of thermal expansion of said circuit board, it is desirable that it is in the condition in which said inorganic filler in said resin constituent was located near said semiconductor device.

[0021] By having made it such a configuration, in a perpendicular direction, the average of the coefficient of thermal expansion of the perpendicular

direction of said resin constituent and the value of the coefficient of thermal expansion of the perpendicular direction of the connection part of said semiconductor device and said circuit board can be maintained almost identically, and the difference of the coefficient of thermal expansion by the side of said semiconductor device and said circuit board can be eased in the direction of a flat surface with said resin constituent from which a coefficient of thermal expansion changes perpendicularly. Therefore, a perpendicular direction and the direction of a flat surface are enabled to prevent effectively generating of the thermal stress by heat expansion of said resin constituent, and when the coefficients of thermal expansion of said semiconductor device and said circuit board differ, the mounting object of a reliable semiconductor device can be acquired.

[0022] Furthermore, it is desirable to have said resin constituent with which the rate of said resin and said inorganic filler was adjusted so that the average of the vertical coefficient of thermal expansion to said circuit board of said resin constituent and the value of the vertical coefficient of thermal expansion to said circuit board of the connection part of said semiconductor device and said circuit board may be mostly in agreement. It is also desirable that the spherical inorganic filler is used as said inorganic filler in said resin constituent.

[0023] Moreover, it is also desirable that said semiconductor device is mounted in said circuit board using a solder bump, that said semiconductor device is mounted in said circuit board using electroconductive glue, and that said semiconductor device is mounted in said circuit board using a projection electrode and electroconductive glue.

[0024]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained based on a drawing. Drawing 1 shows process drawing about the mounting approach of the semiconductor device concerning the first operation gestalt of this invention. As for resin and 9, in drawing 1 , the resin constituent with 1 [ liquefied / a semiconductor device, the joint according / 2 / 3 / a terminal electrode and / 6 / to electroconductive glue in electroconductive glue and 4, and 7 ] according [ the circuit board and 5 ] to a connection electrode and 8 are [ an inorganic filler and 10 ] the resin constituents after hardening. Hereafter, based on process drawing of drawing 1 , the mounting approach of the semiconductor device concerning this first operation gestalt is explained.

[0025] First, as shown in drawing 1 (a), electroconductive glue 3 is beforehand formed in the terminal electrode 2 of a semiconductor device 1. In this case, electroconductive glue 3 may be directly

formed on the terminal electrode 2, and may be formed on the projection electrode (bump) beforehand formed in the terminal electrode 2.

[0026] Next, as shown in drawing 1 (b), this semiconductor device 1 is made a face down (facing down), alignment is performed to the position of the connection electrode 5 of the circuit board 4 (for example, GARAEPO substrate), and a semiconductor device 1 is carried on the circuit board 4. Thereby, the terminal electrode 2 of a semiconductor device 1 and the connection electrode 5 of the circuit board 4 are electrically connected by the joint 6 by electroconductive glue. In this case, the coefficient of thermal expansion of a semiconductor device 1 is smaller than the coefficient of thermal expansion of the circuit board 4.

[0027] Next, as shown in drawing 1 (c), the gap of a semiconductor device 1 and the circuit board 4 is filled up with the liquefied resin constituent 7. And as shown in drawing 1 (d), the liquefied resin constituent 7 is stiffened by turning the circuit board 4 over and heating at the temperature of about 150 degrees C. If it does so, the inorganic filler 9 can obtain the resin constituent 10 after hardening in the condition of having sedimented to the semiconductor device 1 side, in the liquefied resin constituent 7 according to the specific gravity difference of resin 8 (for example, epoxy resin) and the inorganic filler 9 (for example, silica).

[0028] According to the above process, the mounting object of the semiconductor device 1 as shown in drawing 2 can be acquired. In the liquefied resin constituent 7 used at this time, resin 8 and the inorganic filler 9 contain at least. Moreover, as this resin constituent 7, that to which the rate of resin 8 and the inorganic filler 9 is adjusted is used so that the coefficient of thermal expansion of the resin constituent 10 after hardening may be in agreement with the coefficient of thermal expansion of the joint 6 of electroconductive glue. For this reason, even if it is in the condition in which the inorganic filler 9 sedimented in the resin constituent 10 after hardening, the coefficient of thermal expansion of the perpendicularly the resin constituent 10 after hardening averaged is in agreement with the coefficient of thermal expansion of the perpendicular direction of the joint 6 of electroconductive glue.

[0029] Moreover, in the above-mentioned process, since it was made to harden where the inorganic filler 9 is brought near by the semiconductor device 1 side, by the semiconductor device 1 side with a small coefficient of thermal expansion, the coefficient of thermal expansion of the direction of a flat surface of the resin constituent 10 after hardening is small, and as it said that it was large, it has the inclination of a coefficient of thermal

expansion perpendicularly in the resin constituent 10 after hardening by the circuit board 4 side with a large coefficient of thermal expansion.

[0030] Therefore, when using a semiconductor device 1 at an elevated temperature, generating of the thermal stress of the perpendicular direction by the thermal expansion of the resin constituent 10 after hardening which exists in the gap of a semiconductor device 1 and the circuit board 4, and the direction of a flat surface can be prevented. Consequently, the mounting object of the reliable semiconductor device 1 of electric connection can be acquired.

[0031] Moreover, by making it the above configuration, in case it returns to ordinary temperature after carrying out heat hardening of the liquefied resin constituent 7, generating of the thermal stress of the perpendicular direction by the heat shrink of the resin constituent 10 after hardening and the direction of a flat surface can be prevented. Therefore, the dependability of the electric connection at the time of mounting a semiconductor device 1 in the circuit board 4 improves.

[0032] Drawing 3 shows the mounting object of the semiconductor device concerning the second operation gestalt of this invention. As for the joint according [ accord / the circuit board and 5 / a connection electrode / 1 / 2 / a semiconductor device and / 6 ] to electroconductive glue in a terminal electrode and 4, and 10, in drawing 3 , the resin constituent after hardening and 11 are projection electrodes.

[0033] The mounting object of the semiconductor device concerning this second operation gestalt is considered as the configuration which formed the projection electrode 11 in the terminal electrode 2 of a semiconductor device 1. Other configurations are the same as that of the operation gestalt of the above first substantially. Au etc. is used as an ingredient of the projection electrode 11. If it is the configuration which formed the projection electrode 11 in the terminal electrode 2 as shown in this second operation gestalt, in addition to the effectiveness of the operation gestalt of the above 1st, the breadth of the electroconductive glue at the time of mounting a semiconductor device 1 in the circuit board 4 can be regulated, and it will become joinable in a detailed pitch.

[0034] Drawing 4 shows the mounting object of the semiconductor device concerning the third operation gestalt of this invention. In drawing 4 , 1 is a semiconductor device and a joint according [ accord / a connection electrode and 10 / the resin constituent after hardening / 2 / 4 / a terminal electrode and / 12 ] to solder in the circuit board and 5.

[0035] The mounting object of the

semiconductor device concerning this third operation gestalt is considered as the configuration which mounted the terminal electrode 2 of a semiconductor device 1 in the terminal electrode 5 of the circuit board 4 by the joint 12 by solder. Other configurations are the same as that of the operation gestalt of the above first to a real enemy.

[0036] If it is the configuration which mounts a semiconductor device 1 in the circuit board 4 using the joint 12 by solder as shown in this third operation gestalt, in addition to the effectiveness of the operation gestalt of the above 1st, a semiconductor device 1 can be more firmly mounted in the circuit board 4. Moreover, by the mounting approach by the conventional solder, although the quality of the material of the circuit board was limited to the thing (for example, ceramic substrate) near the coefficient of thermal expansion of a semiconductor device on the problem of thermal stress, according to this operation gestalt, it becomes possible to use the circuit board of all the quality of the materials.

[0037] Moreover, in the above operation gestalt [ first ], the second operation gestalt, and the third operation gestalt, although the configuration which made the inorganic filler 9 in a resin constituent sediment to a semiconductor device 1 side was explained supposing the case where the coefficient of thermal expansion of the circuit board 4 is larger than the coefficient of thermal expansion of a semiconductor device 1, this invention is not limited to this. When the coefficient of thermal expansion of the circuit board 4 is smaller than the coefficient of thermal expansion of a semiconductor device 1 (relation contrary to this operation gestalt), it is good, and this configuration can be easily obtained by making it harden without turning the circuit board 4 over, the configuration which made the inorganic filler 9 in a resin constituent sediment to a circuit board 4 side, then in case a liquefied resin constituent is hardened.

[0038]

[Effect of the Invention] According to the mounting approach of the semiconductor device concerning this invention, when producing the mounting object of a semiconductor device and the process changed into an ordinary temperature -- condition from an elevated-temperature condition is performed, generating of the thermal stress of the perpendicular direction by the heat shrink of a resin constituent and the direction of a flat surface can be prevented. therefore, a semiconductor device -- the circuit board -- dependability -- it can mount highly.

[0039] Moreover, according to the mounting object of the semiconductor device concerning this invention, when using the mounting object of this semiconductor device in the state of an

elevated temperature, even if it is, generating of the thermal stress of the perpendicular direction by the thermal expansion of a resin constituent and the direction of a flat surface can be prevented. Therefore, the mounting object of a semiconductor device becomes what has high dependability.

## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] Process drawing showing the mounting approach of the semiconductor device concerning the first operation gestalt of this invention

[Drawing 2] The important section sectional view of the mounting object of the semiconductor device concerning the first operation gestalt of this invention

[Drawing 3] The important section sectional view of the mounting object of the semiconductor device concerning the second operation gestalt of this invention

[Drawing 4] The important section sectional view of the mounting object of the semiconductor device concerning the third operation gestalt of this invention

[Drawing 5] The important section sectional view of the mounting object of the semiconductor device in the conventional technique

[Description of Notations]

1 Semiconductor Device
2 Terminal Electrode
3 Electroconductive Glue
4 Circuit Board
5 Connection Electrode
6 Joint by Electroconductive Glue
7 Liquefied Resin Constituent
8 Resin
9 Inorganic Filler
10 Resin Constituent after Hardening
11 Projection Electrode
12 13 Joint by solder
14 Closure Resin

[첨부그림 1]

Cited Reference

(19)日本国特許庁（JP）　(12)公開特許公報（A）　(11)特許出願公開番号
特開平9－266229
(43)公開日　平成9年(1997)10月7日

| (51)Int.Cl.* | | 識別記号 | 庁内整理番号 | FI | | | 技術表示箇所 |
|---|---|---|---|---|---|---|---|
| H01L | 21/60 | 311 | | H01L | 21/60 | 311S | |
| | 21/56 | | | | 21/56 | R | |
| | 23/29 | | | H05K | 1/18 | J | |
| | 23/31 | | | H01L | 23/30 | Z | |
| H05K | 1/18 | | | | | | |

審査請求　未請求　請求項の数21　OL　(全 6 頁)

(21)出願番号　特願平8－73874

(22)出願日　平成8年(1996)3月28日

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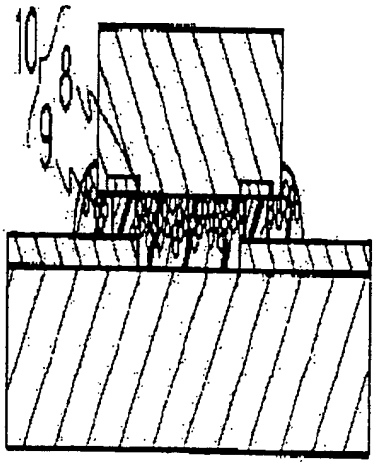
(54)【発明の名称】　半導体装置の実装方法および半導体装置の実装体

【課題】　半導体装置をフェースダウンで回路基板に実装した半導体装置の実装体において、半導体装置と回路基板との電気的接続の信頼性を向上させる。
【解決手段】　半導体装置が回路基板に実装され、半導体装置と回路基板との間隙に樹脂８と無機フィラー９とを含む樹脂組成物１０が備えられ、樹脂組成物１０中の無機フィラー９が熱膨張係数の小さい部材の近傍に位置した構成である。



[청부그림 2]

【特許請求の範囲】

【請求項１】　半導体装置をフェースダウンで回路基板に実装する半導体装置の実装方法であって、前記半導体装置を前記回路基板に実装する工程と、前記半導体装置と前記回路基板との間隙に樹脂と無機フィラーとを含む液状の樹脂組成物を充填する工程と、前記無機フィラーが熱膨張係数の小さい部材の近傍に位置する状態で前記樹脂組成物を硬化する工程とを有することを特徴とする半導体装置の実装方法。

【請求項２】　前記半導体装置の熱膨張係数が前記回路基板の熱膨張係数よりも大きい場合には、前記無機フィラーが前記回路基板の近傍に位置する状態で前記樹脂組成物を硬化する請求項１記載の半導体装置の実装方法。

【請求項３】　前記半導体装置の熱膨張係数が前記回路基板の熱膨張係数よりも小さい場合には、前記無機フィラーが前記半導体装置の近傍に位置する状態で前記樹脂組成物を硬化ずる請求項１記載の半導体装置の実装方法。

【請求項４】　前記無機フィラーの位置決めを行う方法として、前記液状の樹脂組成物中の前記樹脂と前記無機フィラーとの比重差を利用する請求項１，２または3記載の半導体装置の実装方法。

【請求項５】　前記無機フィラーを前記半導体装置の近傍に位置させる方法として、前記回路基板を表返して前記樹脂と前記無機フィラーとの比重差を利用する請求項3記載の半導体装置の実装方法。

【請求項６】　前記無機フィラーの位置決めを行う方法として、前記液状の樹脂組成物中の前記樹脂の粘度が高温状態で急激に下がる性質を利用する請求項１から５のいずれか１項記載の半導体装置の実装方法。

【請求項７】　前記無機フィラーの位置決めと、前記液状の樹脂組成物の硬化とを同一の工程で行う請求項6記載の半導体装置の実装方法。

【請求項８】　前記半導体装置を半田バンプを用いて前記回路基板に実装する請求項１から７のいずれか１項記載の半導体装置の実装方法。

【請求項９】　前記半導体装置を導電性接着剤を用いて前記回路基板に実装する請求項１から７のいずれか１項記載の半導体装置の実装方法。

【請求項１０】　前記半導体装置を突起電極と導電性接着剤とを用いて前記回路基板に実装する請求項１から7のいずれか１項記載の半導体装置の実装方法。

【請求項１１】　半導体装置が回路基板に実装され、前記半導体装置と前記回路基板との間隙に樹脂と無機フィラーとを含む樹脂組成物が備えられ、前記樹脂組成物中の前記無機フィラーが熱膨張係数の小さい部材の近傍に位置した状態であることを特徴とする半導体装置の実装体。

【請求項１２】　熱膨張係数が前記回路基板に対して垂直方向に変化する前記樹脂組成物が備えられている請求項１１記載の半導体装置の実装体。

【請求項１３】　前記半導体装置の熱膨張係数が前記回路基板の熱膨張係数よりも大きい場合には、前記樹脂組成物中の前記無機フィラーが前記回路基板の近傍に位置した状態である請求項１１または１２記載の半導体装置の実装体。

【請求項１４】　前記半導体装置の熱膨張係数が前記回路基板の熱膨張係数よりも小さい場合には、前記樹脂組成物中の前記無機フィラーが前記半導体装置の近傍に位置した状態である請求項１１または１２記載の半導体装置の実装体。

【請求項１５】　前記樹脂組成物の前記回路基板に対する垂直方向の熱膨張係数の平均値が、前記半導体装置と前記回路基板との接続部分の前記回路基板に対する垂直方向の熱膨張係数の値とほぼ一致している請求項１２，１３または１４記載の半導体装置の実装体。

【請求項１６】　前記樹脂組成物の前記回路基板に対する垂直方向の熱膨張係数の平均値と、前記半導体装置と前記回路基板との接続部分の前記回路基板に対する垂直方向の熱膨張係数の値とがほぼ一致するように、前記樹脂と前記無機フィラーとの割合が調整された前記樹脂組成物が備えられている請求項１５記載の半導体装置の実装体。

【請求項１７】　前記樹脂組成物中の前記無機フィラーとして、球状の無機フィラーを用いた請求項１１から１６のいずれか１項記載の半導体装置の実装体。

【請求項１８】　前記半導体装置が半田バンプを用いて前記回路基板に実装されている請求項１１から１７のいずれか１項記載の半導体装置の実装体。

【請求項１９】　前記半導体装置が導電性接着剤を用いて前記回路基板に実装されている請求項１１から１７のいずれか１項記載の半導体装置の実装体。

【請求項２０】　前記半導体装置が突起電極と導電性接着剤とを用いて前記回路基板に実装されている請求項１１から１７のいずれか1項記載の半導体装置の実装体。

【請求項２１】　熱膨張係数の異なる前記半導体装置と前記回路基板とが備えられている請求項１１から２０のいずれか１項記載の半導体装置の実装体。

【発明の詳細な説明】

【発明の属する技術分野】本発明は、半導体装置に関し、詳しくは半導体装置の実装方法およびその実装体に関するものである。

【０００２】

【従来の技術】従来、半導体装置を回路基板上へ実装する場合には、半田付けによる方法が一般的である。しかし、近年、半導体装置のパッケージの小型化と接続端子数の増加により、接続端子間の間隔が狭くなり、従来の半田付け技術によって対処することが次第に困難になってきている。

[첨부그림 3]

【０００３】そこで、最近では、裸の半導体装置を回路基板上に直付けすることによって、実装面積の小型化と効率的使用とを図ろうとする方法が考え出されている。その一例として次のようなものがある。

【０００４】その方法は、まず、半導体装置を回路基板に電気的に接続する際に、半導体装置の端子電極上にあらかじめ硬き金属や拡散防止金属の高き膜と、メッキによって形成された半田層とを積層させる。そして、次に、以上の電極構造を有する半導体装置を回路基板上にフェースダウンさせ、高温に加熱して半導体装置の端子電極上の半田を回路基板の接続電極に融着させるというものである。

【０００５】この方法によれば、接続を一括して行うことができ、さらに、この方法による実装構造は、接続後の機械的強度が強いという特徴を有する。したがって、この方法は、有効な方法であるとされている。

【０００６】また、米国特許第５１２１１９０号明細書には、半田による接合部の安定性を確保するために、半導体装置と回路基板との間を樹脂封止した半導体装置の実装体が開示されている。

【０００７】以下、従来の半導体装置の実装方法とその実装体について説明する。図５は、従来技術における半導体装置の実装体の要部断面図である。図５において、１は半導体装置、２は半導体装置１の端子電極、４は回路基板、５は接続電極、１３は半田による接合部、１４は封止樹脂である。

【０００８】この従来技術においては、まず、端子電極２上に半田バンプが形成された半導体装置１を、回路基板４の接続端子５の所定の位置に、フェースダウンで搭載する。次に、２００～３００℃の高温に加熱して、端子電極２上の半田バンプを溶融させ接続端子５に融着させる。こうすることにより、半導体装置１と回路基板４とが半田による接合部１３により接続される。その後、半導体装置１と回路基板４との間隙に液状の封止樹脂１４を充填し、１５０℃程度の温度で加熱硬化する。以上の工程により、半導体装置１を封止樹脂１４で封止した実装体を得ることができる。

【０００９】

【発明が解決しようとする課題】しかしながら、以上の従来の半導体装置の実装体においては、この半導体装置の実装体を使用する際の環境温度の変化により、半導体装置１と回路基板４との熱膨張係数の差による熱応力が生じ、その熱応力が半田による接合部１３に加わることとなる。また、この半導体装置の実装体を特に高温領域で使用する場合には、半導体装置１と回路基板４との間隙に充填されている封止樹脂１４においても熱膨張による新たな熱応力が生じ、この熱応力も半田による接合部１３に加わることとなる。したがって、この従来の実装体においては、これらの熱応力がすべて半田による接合部１３に加わるので、半導体装置１と回路基板４との電気的接続の信頼性が悪化する。

【００１０】これらの熱応力を避けるためには、封止樹脂１４として熱膨張係数の小さなもの（さらに好ましくは半田による接合部１３の熱膨張係数に一致するもの）を用いて、半田による接合部１３の安定性を確保する必要がある。このような（熱膨張係数の小さい）封止樹脂１４としては、封止樹脂１４中に無機フィラーを約４０～７５重量％（さらに好ましくは約５０～６０重量％）含有させたものが考えられる。

【００１１】しかし、このような封止樹脂１４（半田による接合部１３の熱膨張係数に合致する程に小さい熱膨張係数を有するもの）を用いると、回路基板に対して垂直方向（以下、単に「垂直方向」ともいう。）に働く半田による接合部１３の熱応力については解決するが、回路基板に沿って平行方向（以下、「平面方向」という。）に働く半導体装置１と回路基板４との熱膨張係数の差によって生ずる熱応力については解決できない。そればかりか、このような封止樹脂１４を用いると、平面方向の熱応力は一層増大する。

【００１２】このような平面方向の熱応力の増大は、半田による接合部１３と半導体装置１および回路基板４との熱膨張係数が大きく異なることにより生ずる。つまり、封止樹脂１４の熱膨張係数を半田の接合部１３に合致させたとしても、半導体装置１および回路基板４の熱膨張係数とは合致させることができないので、その熱膨張係数の差によって熱応力の増大が起こるのである。したがって、これら平面方向の熱膨張係数の差により生ずる熱応力が、半田による接合部１３へ加わり、半導体装置１と回路基板４との電気的接続の信頼性を悪化させる。

【００１３】本発明は、このような課題を解決するためになされたもので、信頼性の高い半導体装置の実装体と、これを得るための半導体装置の実装方法を提供することを目的とする。

【００１４】

【課題を解決するための手段】上記目的を達成するための本発明は、半導体装置をフェースダウンで回路基板に実装する半導体装置の実装方法であって、前記半導体装置を前記回路基板に実装する工程と、前記半導体装置と前記回路基板との間隙に樹脂と無機フィラーとを含む液状の樹脂組成物を充填する工程と、前記無機フィラーが熱膨張係数の小さい部材の近傍に位置する状態で前記樹脂組成物を硬化する工程とを有することを特徴とする。

【００１５】こうすることにより、前記半導体装置と前記回路基板との間に介在する硬化性の前記樹脂組成物においては、前記無機フィラーの分布状態、つまり前記無機フィラーの在る部分と無い部分との間で熱膨張係数の傾きが発生することとなる。したがって、前記無機フィラーを如何に分布させるかにより、前記樹脂組成物の熱膨張による熱応力の発生を、垂直方向および平面方向と

[첨부그림 4]

もに効果的に防止することができる。

【００１６】また、前記半導体装置の熱膨脹係数が前記回路基板の熱膨脹係数よりも大きい場合には、前記無機フィラーが前記回路基板の近傍に位置する状態で前記樹脂組成物を硬化することが好ましい。ここで前記無機フィラーは、熱伝導性を向上させる効果を有するので、前記実装方法によれば前記回路基板に対する熱伝導が向上し、前記半導体装置と前記回路基板の熱膨脹係数の差が緩和される。したがって、硬化後の前記樹脂組成物は垂直方向に熱膨脹係数の傾きを有することとなり、前記樹脂組成物の熱膨脹による熱応力の発生を垂直方向および平面方向ともに防止することができ、前記半導体装置と前記回路基板とを信頼性高く実装することができる。

【００１７】さらに、前記半導体装置の熱膨脹係数が前記回路基板の熱膨脹係数よりも小さい場合には、前記無機フィラーが前記半導体装置の近傍に位置する状態で前記樹脂組成物を硬化することが好ましい。こうすることにより、前記半導体装置に対する熱伝導が向上し、前記半導体装置と前記回路基板の熱膨脹係数の差が緩和され、前記樹脂組成物の熱膨脹による熱応力の発生を垂直方向におよび平面方向ともに防止することができる。

【００１８】また、前記無機フィラーの位置決めを行う方法としては、前記液状の樹脂組成物中の前記樹脂と前記無機フィラーとの比重差を利用する方法、および前記液状の樹脂組成物中の前記樹脂の粘度が高温状態で急激に下がる性質を利用する方法等が好ましい。さらに、前記無機フィラーを前記半導体装置の近傍に位置させる方法として、前記回路基板を高速して前記樹脂と前記無機フィラーとの比重差を利用する方法も好ましい。また、前記無機フィラーの位置決めと、前記液状の樹脂組成物の硬化とを同一の工程で行う方法も好ましい。

【００１９】さらに、前記半導体装置を半田バンプを用いて前記回路基板に実装する方法、前記半導体装置を導電性接着剤を用いて前記回路基板に実装する方法、および前記半導体装置を突起電極と導電性接着剤とを用いて前記回路基板に実装する方法等も好ましい。

【００２０】また、本発明に係る半導体装置に実装体は、半導体装置が回路基板に実装され、前記半導体装置と前記回路基板との間隙に樹脂と無機フィラーとを含む樹脂組成物が備えられ、前記樹脂組成物中の前記無機フィラーが熱膨脹係数の小さい部材の近傍に位置した状態であることを特徴とする。さらに、熱膨脹係数が前記回路基板に対して垂直方向に変化する前記樹脂組成物が備えられていることが好ましい。また、前記半導体装置の熱膨脹係数が前記回路基板の熱膨脹係数よりも大きい場合には、前記樹脂組成物中の前記無機フィラーが前記回路基板の近傍に位置した状態であること、および前記半導体装置の熱膨脹係数が前記回路基板の熱膨脹係数よりも小さい場合には、前記樹脂組成物中の前記無機フィラーが前記半導体装置の近傍に位置した状態であることが好ましい。

【００２１】このような構成にしたことにより、垂直方向においては、前記樹脂組成物の垂直方向の熱膨張係数の平均値と、前記半導体装置と前記回路基板との接続部分の垂直方向の熱膨張係数の値とをほぼ同一に維持することができ、平面方向においては、垂直方向に熱膨脹係数が変化する前記樹脂組成物によって、前記半導体装置側と前記回路基板側との熱膨脹係数の差を緩和することができる。したがって、前記樹脂組成物の熱膨脹による熱応力の発生を垂直方向および平面方向ともに効果的に防止することが可能となり、前記半導体装置と前記回路基板の熱膨脹係数が異なる場合においても、信頼性の高い半導体装置の実装体を得ることができる。

【００２２】さらに、前記樹脂組成物の前記回路基板に対する垂直方向の熱膨脹係数の平均値と、前記半導体装置と前記回路基板との接続部分の前記回路基板に対する垂直方向の熱膨脹係数の値とがほぼ一致するように、前記樹脂と前記無機フィラーとの割合が調整された前記樹脂組成物が備えられていることが好ましい。前記樹脂組成物中の前記無機フィラーとしては、球状の無機フィラーが用いられていることも好ましい。

【００２３】また、前記半導体装置が半田バンプを用いて前記回路基板に実装されていること、前記半導体装置が導電性接着剤を用いて前記回路基板に実装されていること、および前記半導体装置が突起電極と導電性接着剤とを用いて前記回路基板に実装されていることも好ましい。

【００２４】

【発明の実施の形態】以下、本発明の実施の形態について、図面に基づいて説明する。図１は、本発明の第一の実施形態に係る半導体装置の実装方法についての工程図を示している。図１において、１は半導体装置、２は端子電極、３は導電性接着剤、４は回路基板、５は接続電極、６は導電性接着剤による接合部、７は液状の樹脂組成物、８は樹脂、９は無機フィラー、１０は硬化後の樹脂組成物である。以下、図１の工程図に基づいて、この第一の実施形態に係る半導体装置の実装方法について説明する。

【００２５】まず、図１（ａ）に示すように、半導体装置１の端子電極２にあらかじめ導電性接着剤３を形成する。この場合、導電性接着剤３は、端子電極２の上に直接形成してもよいし、端子電極２にあらかじめ形成した突起電極（バンプ）の上に形成してもよい。

【００２６】次に、図１（ｂ）に示すように、この半導体装置１をフェースダウン（下向き）にして回路基板４（例えばガラエポ基板）の接続電極５の所定の位置に位置合わせを行い、回路基板４の上に半導体装置１を搭載する。これにより、半導体装置１の端子電極２と回路基板４の接続電極５とが導電性接着剤による接合部６によって電気的に接続される。この場合、半導体装置１の熱

[첨부그림 5]

膨張係数は回路基板４の熱膨張係数よりも小さい。

【００２７】次に、図１（ｃ）に示すように、半導体装置１と回路基板４との間隙に液状の樹脂組成物７を充填する。そして、図１（ｄ）に示すように、回路基板４を表退して１５０℃程度の温度で加熱することにより液状の樹脂組成物７を硬化させる。そうすると、液状の樹脂組成物７中で、樹脂８（例えばエポキシ樹脂）と無機フィラー９（例えばシリカ）との比重差によって無機フィラー９が半導体装置１側に沈降した状態での硬化後の樹脂組成物１０を得ることができる。

【００２８】以上の工程により、図２に示すような半導体装置１の実装体を得ることができる。このとき用いられる液状の樹脂組成物７には、少なくとも樹脂８と無機フィラー９とが含有されている。またこの樹脂組成物７としては、硬化後の樹脂組成物１０の熱膨張係数が導電性接着剤の接合部５の熱膨張係数に一致するように、樹脂８と無機フィラー９との割合が調整されているものが用いられる。このため、硬化後の樹脂組成物１０中で無機フィラー９が沈降した状態であっても、硬化後の樹脂組成物１０の平均した垂直方向の熱膨張係数は導電性接着剤の接合部５の垂直方向の熱膨張係数と一致している。

【００２９】また、上記工程においては、無機フィラー９を半導体装置１側に寄せた状態で硬化させたので、硬化後の樹脂組成物１０の平面方向の熱膨張係数は、熱膨張係数の小さい半導体装置１側では小さく、熱膨張係数の大きい回路基板４側では大きいといったように、硬化後の樹脂組成物１０中で垂直方向に熱膨張係数の傾斜を有する。

【００３０】したがって、半導体装置１を高温で使用する場合においても、半導体装置１と回路基板４との間隙に存在する硬化後の樹脂組成物１０の熱膨張による垂直方向および平面方向の熱応力の発生を防止することができる。その結果、電気的な接続の信頼性の高い半導体装置１の実装体を得ることができる。

【００３１】また、以上の構成にすることにより、液状の樹脂組成物７を加熱硬化した後に常温に戻す際においても、硬化後の樹脂組成物１０の熱収縮による垂直方向および平面方向の熱応力の発生を防止することができる。したがって、半導体装置１を回路基板４に実装する際の電気的な接続の信頼性が向上する。

【００３２】図３は、本発明の第二の実施形態に係る半導体装置の実装体を示している。図３において、１は半導体装置、２は端子電極、４は回路基板、５は接続電極、６は導電性接着剤による接合部、１０は硬化後の樹脂組成物、１１は突起電極である。

【００３３】この第二の実施形態に係る半導体装置の実装体は、半導体装置１の端子電極２に突起電極１１を設けた構成としている。その他の構成は、実質的に上記第一の実施形態と同様である。突起電極１１の材料としては、Ａｕ等を用いる。この第二の実施形態に示したように、端子電極２に突起電極１１を設けた構成とすると、上記第１の実施形態の効果に加えて、半導体装置１を回路基板４に実装する際の導電性接着剤の広がりを規制することができ、微細ピッチでの接合が可能となる。

【００３４】図４は、本発明の第三の実施形態に係る半導体装置の実装体を示している。図４において、１は半導体装置、２は端子電極、４は回路基板、５は接続電極、１０は硬化後の樹脂組成物、１２は半田による接合部である。

【００３５】この第三の実施形態に係る半導体装置の実装体は、半導体装置１の端子電極２を回路基板４の端子電極５に半田による接合部１２で実装した構成としている。その他の構成は、実質的に上記第一の実施形態と同様である。

【００３６】この第三の実施形態に示したように、半田による接合部１２を用いて半導体装置１を回路基板４に実装する構成とすると、上記第１の実施形態の効果に加えて、半導体装置１を回路基板４に、より強固に実装することができる。また、従来の半田による実装方法では、熱応力の問題で回路基板の材質が半導体装置の熱膨張係数に近いもの（例えば、セラミック基板）に限定されていたが、本実施形態によれば、あらゆる材質の回路基板を用いることが可能となる。

【００３７】また、以上の第一の実施形態、第二の実施形態および第三の実施形態においては、半導体装置１の熱膨張係数よりも回路基板４の熱膨張係数の方が大きい場合を想定して、樹脂組成物中の無機フィラー９を半導体装置１側に沈降させた構成について説明したが、本発明はこれに限定されるものではない。半導体装置１の熱膨張係数よりも回路基板４の熱膨張係数の方が小さい場合（本実施形態と逆の関係）には、樹脂組成物中の無機フィラー９を回路基板４側に沈降させた構成とすればよく、この構成は、液状の樹脂組成物の硬化を行う際に、回路基板４を表退させずに硬化させることによって容易に得ることができる。

【００３８】

【発明の効果】本発明に係る半導体装置の実装方法によれば、半導体装置の実装体を生産する際に高温状態から常温状態にする工程を行った場合においても、樹脂組成物の熱収縮による垂直方向および平面方向の熱応力の発生を防止することができる。したがって、半導体装置を回路基板に信頼性高く実装することができる。

【００３９】また、本発明に係る半導体装置の実装体によれば、この半導体装置の実装体を高温状態で使用する場合にあっても、樹脂組成物の熱膨張による垂直方向および平面方向の熱応力の発生を防止することができる。したがって、半導体装置の実装体は信頼性の高いものとなる。

【図面の簡単な説明】

[첨부그림 6]

【図１】本発明の第一の実施形態に係る半導体装置の実装方法を示す工程図

【図２】本発明の第一の実施形態に係る半導体装置の実装体の要部断面図

【図３】本発明の第二の実施形態に係る半導体装置の実装体の要部断面図

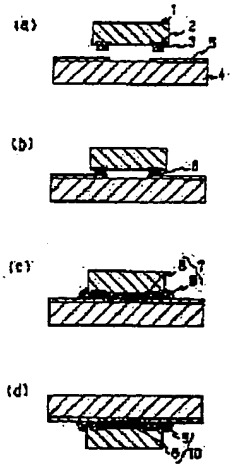
【図４】本発明の第三の実施形態に係る半導体装置の実装体の要部断面図

【図５】従来技術における半導体装置の実装体の要部断面図

【符号の説明】

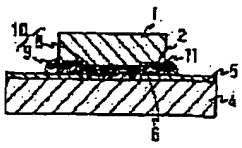
１　半導体装置
２　端子電極
３　導電性接着剤
４　回路基板
５　接続電極
６　導電性接着剤による接合部
７　液状の樹脂組成物
８　樹脂
９　無機フィラー
１０　硬化後の樹脂組成物
１１　突起電極
１２，１３　半田による接合部
１４　封止樹脂

【図１】

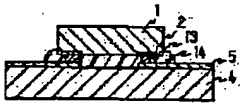



【図２】

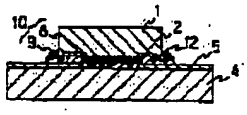
【図３】



【図５】



【図４】



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